Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

DDC S9700-53DX Programming Guide

Revision 1.0

The information contained in this document is considered confidential information and should not be disclosed without prior consent of UfiSpace. This information is considered preliminary and may change in substance or form prior to final product release.

Jan. 30, 2020
UfiSpace Technology Corporation
Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

Revision History

Date	Rev	Author	Summary of Change
Jan 30, 2020	R1.0	Ken Chen	First Draft Release.

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

Table of Contents

1 Overview....4
1.1 Physical Overview....4
1.2 Feature Summary....5
1.3 Mechanical Outline....6
1.4 Front & Real Panel Design....6
1.5 LED Indicators....7
1.6 Network Ports....9
1.6.1 Ports Assignment....9
1.6.2 Ports mapping....10
1.7 OOB Ports....13
1.8 Console Port....13
1.9 Interrupt Tree....13
1.9.1 CPLD1 Interrupt....13
1.9.2 CPLD2/3/4/5 Interrupt....14
2 Main System....16
2.1 Memory and I/O Mapping....16
2.1.1 SMbus....20
3 BMC sub-system....26
3.1 LPC....26
3.2 GPIO....27
3.3 Base Board Management....28
4 CPLD....30
4.1 CPU board CPLD Register Mapping and Description....30
4.2 Main board CPLD Register Mapping and Description....32

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

1 Overview

This document describes the programming interfaces of the Distributed Disaggregated Chassis Routing System, S9700-53DX, designed for telco service application. The main purpose is to aid in porting software to the hardware platform.

The S9700-53DX is the best of breed robust, flexible and carrier-grade Distributed Disaggregated Chassis (DDC) line card white box router that can be deployed in the core or edge to transport services over a scalable next-gen service provider network. Equipped with 100GE service supports and 400GE fabric ports, the S9700-53DX enables fault and performance monitoring, non-stop routing support for control and data plane, and comprehensive high-availability networks.

The S9700-53DX can be positioned as standalone or coupled with the S9705-48D fabric white box router in small, medium, and large clusters enabling 4Tb to 192Tb switching capacity. By connecting to the S9705-48D (fabric), it scales out not only economically and rapidly, but it also brings down the total cost of ownership.

The DDC Routing System adopts the innovated discrete Network Cloud Processor (NCP) and Network Cloud Fabric (NCF) building blocks providing flexibility to core router needs in the industry, integral to Ethernet switching performance and intelligence to networks while minimizing the network complexity.

1.1 Physical Overview

Front View



Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Rear View



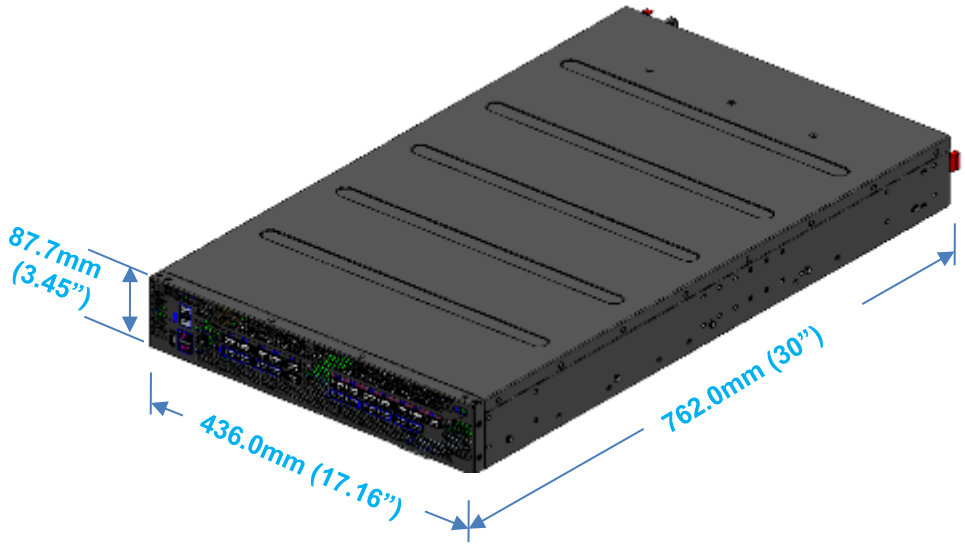
1.2 Feature Summary

- 1+1 Redundant power supply unit
  - 2000W output
  - 90~264VAC/-40~-72VDC input
  - Field replaceable
- 3+1 Redundant fan module
  - 16000 RPM
  - Front to Back air flow
  - Field replaceable
- Ethernet data ports:
  - 40 x 100GE QSFP28 ports
  - 13 x 400GE QSFPDD ports
- Front/Real panel LED indicators:
  - 2 x power status LED
  - 1 x FAN status LED
  - 1 x system status LED
  - Per port link status LED
  - Beaconing LED(2-digits 7 segment)
  - Per port FAN status LED (Rear panel on each FRU)
  - Per port PSU status LED (Rear panel on each FRU)
- Management interfaces:
  - 1 x GE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact router for system reset/reload default configuration
  - 2 x 10GE SFP+ management ports

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

1.3 Mechanical Outline

S9700-53DX is designed to meet cabinet with 19'' depth installation requirement. This 2RU systemmechanical dimension is: 436mm(W) x 762mm(D) x 87.7mm(H)



1.4 Front & Real Panel Design

S9700-53DX front panel IO ports & LED include below functionalities :

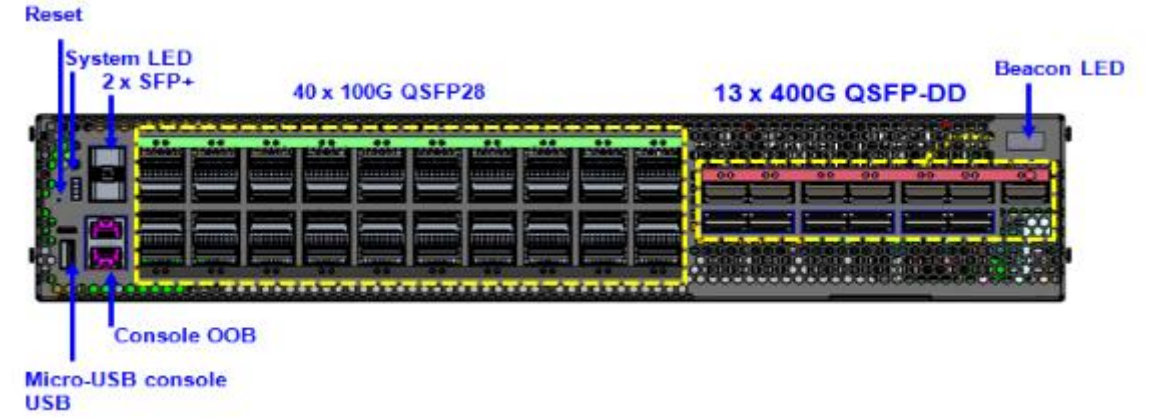
- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ Beacon LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB
- Ethernet data ports
  - ✓ 40x 100GE QSFP28 ports
  - ✓ 13x 400GE QSFPDD ports

S9700-53DX real panel design:

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

- FAN status LED
- PSU status LED

Detailed IO arrangement is shown as below :



1.5 LED Indicators

The system status and stacking LED are placed on main board.

LED Indication	Behavior	Description
SYS	OFF	No power
	Solid Green	Host CPU/BMC is up
	Solid Amber	Power is up but Host CPU/BMC is not up
FAN	OFF	Fans are not initialized
	Solid Green	All Fans are work normal
	Solid Amber	Fan fail : one or more Fans need service
PS1	OFF	No power
	Solid Green	PSU1 is work normal
	Solid Amber	PSU1 fail (PSU1 need service)

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

PS2	OFF	No power
	Solid Green	PSU2 is work normal
	Solid Amber	PSU2 fail (PSU2 need service)

The platform will have 2 green LEDs integrated in the front panel management RJ45 port.

LED Indication	Behavior	Description
OOB	OFF	No power
	Solid Green	1G link-up
	Blinking Green	1G TX/RX activity
	Solid Amber	10M/100M link-up
	Blinking Amber	10M/100M TX/RX activity

The following table shows the 10GE/100GE/400GE LED definitions:

Location	LED Indication	Color	Behavior	Description
SFP+ ports	Link/Act/Speed of 10GE	Green	Solid	Link up
			Blinking	Packet transmitting or receiving
			Off	No link or port disable
QSFP28	Link/Act/Speed	Green	Solid	Link up at 100GE
			Blinking	Packet transmitting or receiving at 100GE
			Off	No link or port disable
		Yellow	Solid	Link up at 40GE
			Blinking	Packet transmitting or receiving at 40GE
			Off	No link or port disable
QSFPDD	Link/Act/Speed	Green	Solid	Link up at 400GE
			Blinking	Packet transmitting or receiving at 400GE
			Off	No link or port disable
		Red	Solid	Identify potential fail port
		Blue	Solid	Management to locate switch

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

1.6 Network Ports

1.6.1 Ports Assignment

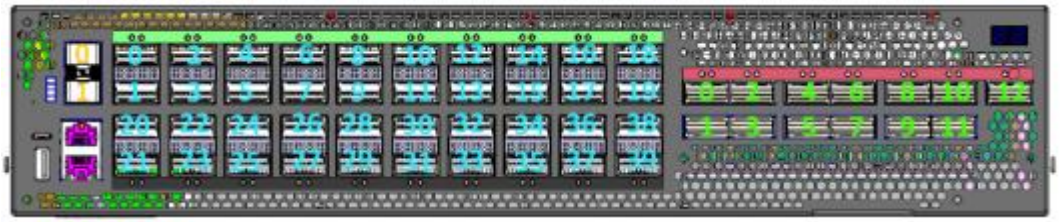


Table below shows the network ports numbering & speed:

Front Panel Port Number	Speed	Notes
P0	10GE/25GE/40GE/100GE	ER4 optics capable
P1	10GE/25GE/40GE/100GE	ER4 optics capable
P2	10GE/25GE/40GE/100GE	ER4 optics capable
P3	10GE/25GE/40GE/100GE	ER4 optics capable
P4	10GE/25GE/40GE/100GE	ER4 optics capable
P5	10GE/25GE/40GE/100GE	ER4 optics capable
P6	10GE/25GE/40GE/100GE	ER4 optics capable
P7	10GE/25GE/40GE/100GE	ER4 optics capable
P8	10GE/25GE/40GE/100GE	ER4 optics capable
P9	10GE/25GE/40GE/100GE	ER4 optics capable
P10	10GE/25GE/40GE/100GE	ER4 optics capable
P11	10GE/25GE/40GE/100GE	ER4 optics capable
P12	10GE/25GE/40GE/100GE	ER4 optics capable
P13	10GE/25GE/40GE/100GE	ER4 optics capable
P14	10GE/25GE/40GE/100GE	ER4 optics capable
P15	10GE/25GE/40GE/100GE	ER4 optics capable
P16	10GE/25GE/40GE/100GE	ER4 optics capable
P17	10GE/25GE/40GE/100GE	ER4 optics capable
P18	10GE/25GE/40GE/100GE	ER4 optics capable
P19	10GE/25GE/40GE/100GE	ER4 optics capable
P20	100GE	ER4 optics capable
P21	100GE	ER4 optics capable
P22	100GE	ER4 optics capable
P23	100GE	ER4 optics capable
P24	100GE	ER4 optics capable
P25	100GE	ER4 optics capable
P26	100GE	ER4 optics capable
P27	100GE	ER4 optics capable
P28	100GE	ER4 optics capable

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

P29	100GE	ER4 optics capable
P30	100GE	ER4 optics capable
P31	100GE	ER4 optics capable
P32	100GE	ER4 optics capable
P33	100GE	ER4 optics capable
P34	100GE	ER4 optics capable
P35	100GE	ER4 optics capable
P36	100GE	ER4 optics capable
P37	100GE	ER4 optics capable
P38	100GE	ER4 optics capable
P39	100GE	ER4 optics capable

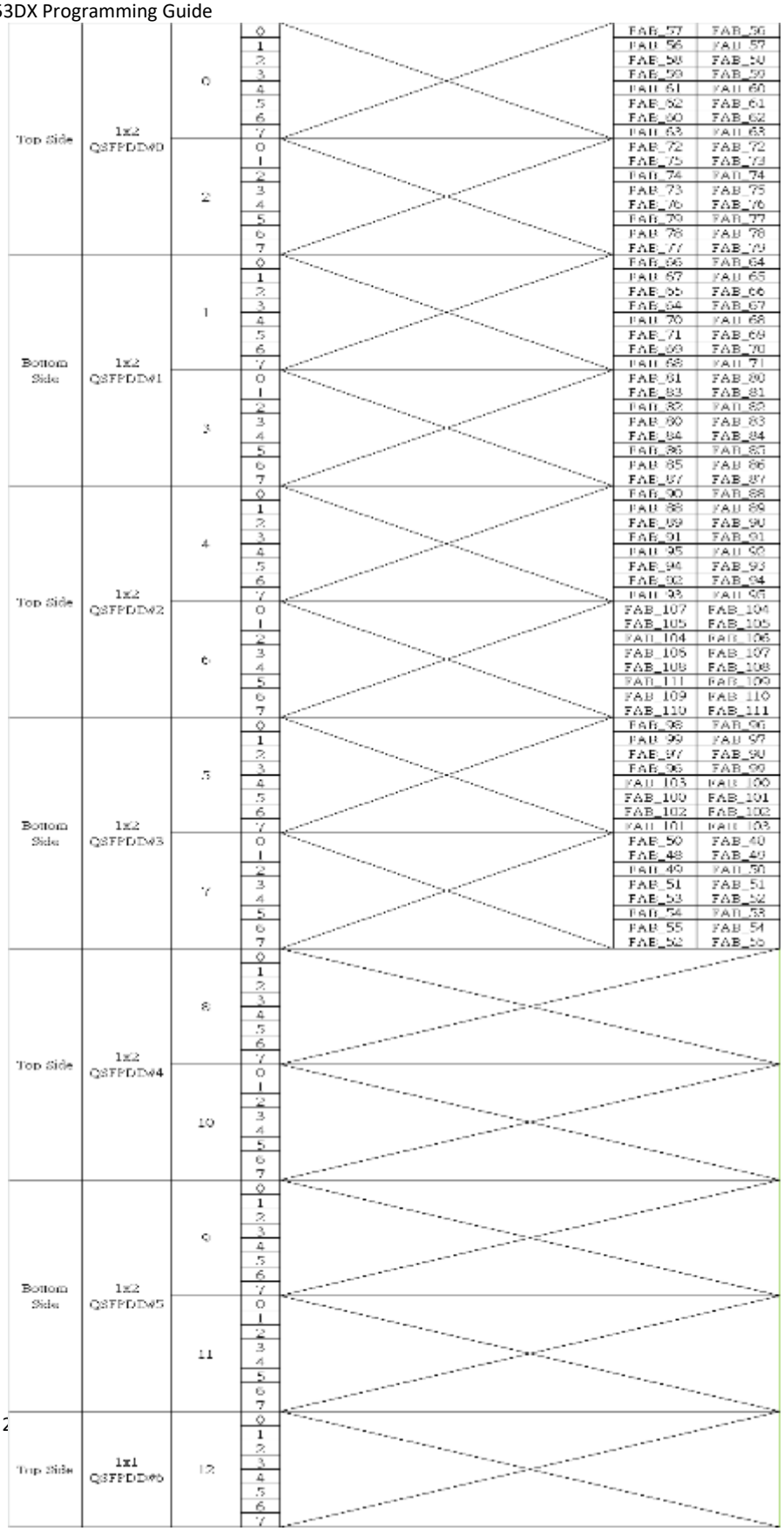
1.6.2 Ports mapping

Front Panel				Reverse Gearbox mode					
				PHY				MAC	
						Line side		Host side	
Connector		Physical port	Lane	MIIM Bus [7:0]	MIIM Address [4:2]	TX_Lane	RX_Lane	TX_Lane (NIF/FAB)	RX_Lane (NIF/FAB)
Top Side	2x1 QSFP28#0	0	0	0	001	0	0	NIF_02	NIF_02
			1			1	1		
			2			2	2	NIF_03	NIF_01
			3			3	3		
		1	0			8	8	NIF_04	NIF_04
			1			9	9		
			2			10	10	NIF_05	NIF_06
			3			11	11		
Bottom Side	2x1 QSFP28#1	20	0			12	12	NIF_06	NIF_07
			1			13	13		
			2			14	14	NIF_07	NIF_05
			3			15	15		
		21	0			4	4	NIF_01	NIF_00
			1			5	5		
			2			6	6	NIF_00	NIF_03
			3			7	7		
Top Side	2x1 QSFP28#2	2	0		010	0	0	NIF_08	NIF_09
			1			1	1		
			2			2	2	NIF_09	NIF_08
			3			3	3		
		3	0			8	8	NIF_12	NIF_14
			1			9	9		
			2			10	10	NIF_13	NIF_12
			3	0		11	11		
Bottom Side	2x1 QSFP28#3	22	0			12	12	NIF_14	NIF_13
			1			13	13		
			2			14	14	NIF_15	NIF_15
			3			15	15		
		24	0			4	4	NIF_10	NIF_10
			1			5	5		
			2			6	6	NIF_11	NIF_11
			3			7	7		
Top Side	2x1 QSFP28#4	4	0		011	0	0	NIF_16	NIF_19
			1			1	1		
			2			2	2	NIF_17	NIF_18
			3			3	3		
		5	0			8	8	NIF_20	NIF_20
			1			9	9		
			2			10	10	NIF_21	NIF_22
			3			11	11		
Bottom Side	2x1 QSFP28#5	24	0			12	12	NIF_22	NIF_21
			1			13	13		
			2			14	14	NIF_23	NIF_23
			3			15	15		
		25	0			4	4	NIF_18	NIF_17
			1			5	5		
			2			6	6	NIF_19	NIF_16
			3			7	7		

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Top Side	2x1 QSFP28#6	6	0		100	0	0	NIF_24	NIF_27
			1			1	1		
			2			2	2	NIF_25	NIF_25
			3			3	3		
		7	0			8	8	NIF_28	NIF_28
			1			9	9		
			2			10	10	NIF_29	NIF_29
			3			11	11		
Bottom Side	2x1 QSFP28#7	26	0			12	12	NIF_30	NIF_30
			1			13	13		
			2			14	14	NIF_31	NIF_31
			3			15	15		
		27	0			4	4	NIF_26	NIF_26
			1			5	5		
			2			6	6	NIF_27	NIF_24
			3			7	7		
Top Side	2x1 QSFP28#8	8	0			0	0	NIF_32	NIF_35
			1			1	1		
			2			2	2	NIF_34	NIF_33
			3			3	3		
		9	0			8	8	NIF_36	NIF_36
			1			9	9		
			2			10	10	NIF_37	NIF_37
			3			11	11		
Bottom Side	2x1 QSFP28#9	28	0	1	101	12	12	NIF_38	NIF_38
			1			13	13		
			2			14	14	NIF_39	NIF_39
			3			15	15		
		29	0			4	4	NIF_33	NIF_32
			1			5	5		
			2			6	6	NIF_35	NIF_34
			3			7	7		
Top Side	2x1 QSFP28#10	10	0		001	0	0	NIF_40	NIF_41
			1			1	1		
			2			2	2	NIF_41	NIF_40
			3			3	3		
		11	0			8	8	NIF_44	NIF_44
			1			9	9		
			2			10	10	NIF_45	NIF_47
			3			11	11		
Bottom Side	2x1 QSFP28#11	30	0			12	12	NIF_46	NIF_46
			1			13	13		
			2			14	14	NIF_47	NIF_45
			3			15	15		
		31	0			4	4	NIF_43	NIF_43
			1			5	5		
			2			6	6	NIF_42	NIF_42
			3			7	7		
Top Side	2x1 QSFP28#12	12	0		010	0	0	NIF_89	NIF_88
			1			1	1		
			2			2	2	NIF_90	NIF_89
			3			3	3		
		13	0			8	8	NIF_95	NIF_92
			1			9	9		
			2			10	10	NIF_94	NIF_93
			3			11	11		
Bottom Side	2x1 QSFP28#13	32	0			12	12	NIF_93	NIF_95
			1			13	13		
			2			14	14	NIF_92	NIF_94
			3			15	15		
		33	0			4	4	NIF_88	NIF_90
			1			5	5		
			2			6	6	NIF_91	NIF_91
			3			7	7		
Top Side	2x1 QSFP28#14	14	0		011	0	0	NIF_81	NIF_81
			1			1	1		
			2			2	2	NIF_82	NIF_80
			3			3	3		
		15	0			8	8	NIF_87	NIF_85
			1			9	9		
			2			10	10	NIF_86	NIF_86
			3			11	11		
Bottom Side	2x1 QSFP28#15	34	0	2		12	12	NIF_85	NIF_87
			1			13	13		
			2			14	14	NIF_84	NIF_84
			3			15	15		
		35	0			4	4	NIF_80	NIF_82
			1			5	5		
			2			6	6	NIF_83	NIF_83
			3			7	7		
Top Side	2x1 QSFP28#16	16	0		100	0	0	NIF_74	NIF_72
			1			1	1		
			2			2	2	NIF_73	NIF_73
			3			3	3		
		17	0			8	8	NIF_79	NIF_77
			1			9	9		
			2			10	10	NIF_78	NIF_76
			3			11	11		
Bottom Side	2x1 QSFP28#17	36	0			12	12	NIF_77	NIF_78
			1			13	13		
			2			14	14	NIF_76	NIF_76
			3			15	15		
		37	0			4	4	NIF_75	NIF_74
			1			5	5		
			2			6	6	NIF_72	NIF_75
			3			7	7		
Top Side	2x1 QSFP28#18	18	0			0	0	NIF_66	NIF_64
			1			1	1		
			2			2	2	NIF_65	NIF_65
			3			3	3		
		19	0			8	8	NIF_70	NIF_71
			1			9	9		
			2			10	10	NIF_71	NIF_70
			3	3	101	11	11		
Bottom Side	2x1 QSFP28#19	38	0			12	12	NIF_68	NIF_69
			1			13	13		
			2			14	14	NIF_69	NIF_68
			3			15	15		
		39	0			4	4	NIF_67	NIF_66
			1			5	5		
			2			6	6	NIF_64	NIF_67
			3			7	7		

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

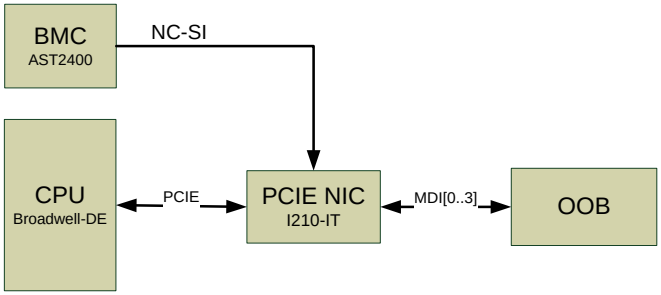


1.7 OOB Ports

The S9700-53DX router includes 1standard GE RJ45 port for out of band (OOB) management, share by CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

PCIe interface is routed between CPU & NIC I210-IT, OOB supports 10/100/1000Mbps operation. NC-SI is connected between BMC & NIC I210-IT, OOB speed is limited to 100Mbps in this case.

OOB to BMC can be disabled by BIOS.



1.8 Console Port

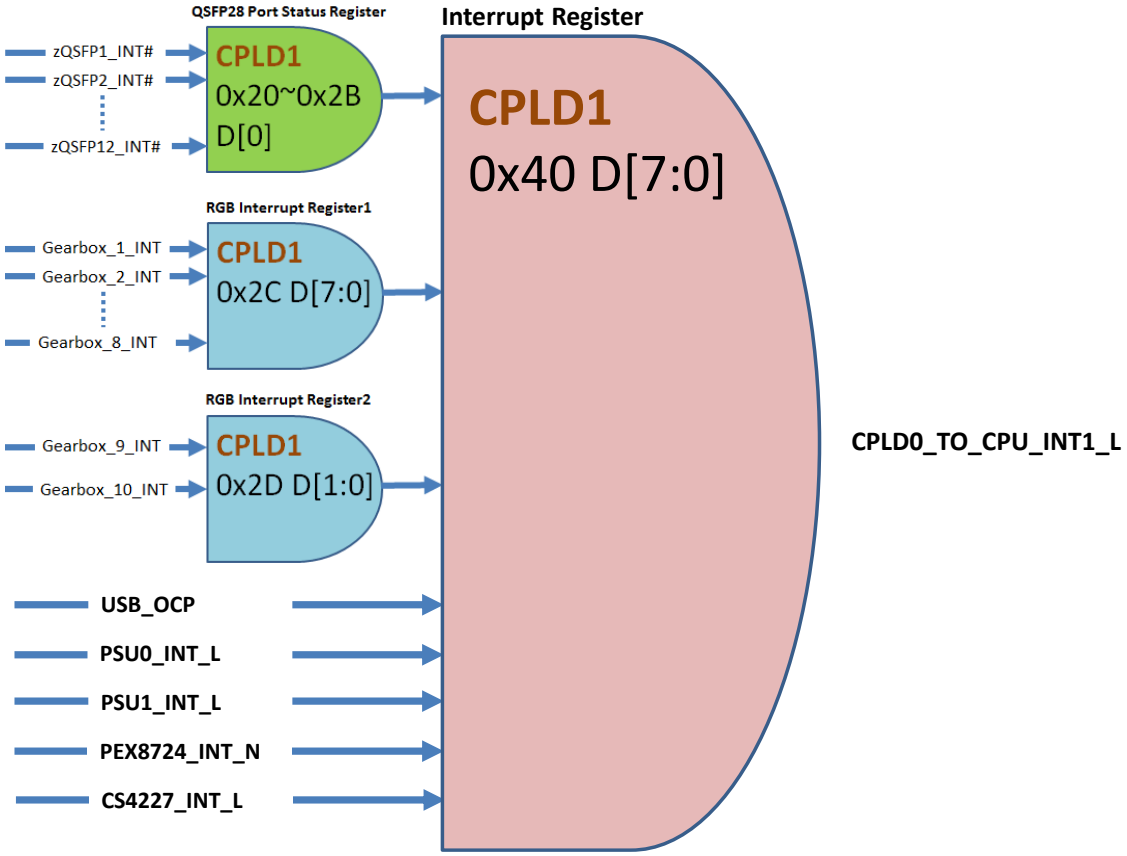
Two console ports available for S9700-53DX systems access, both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown as below. Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The default baud rate is 115200 bps.

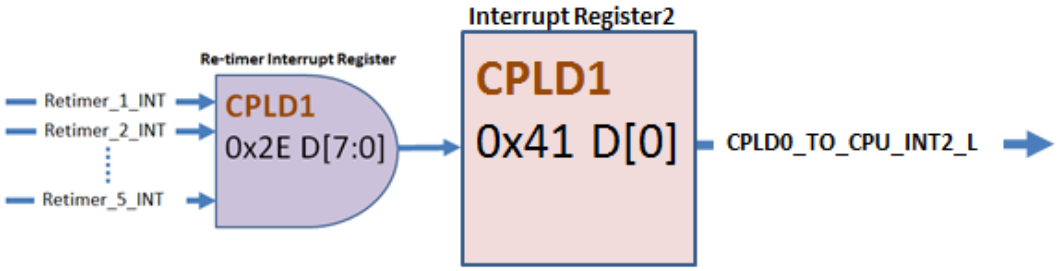
PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

1.9 Interrupt Tree

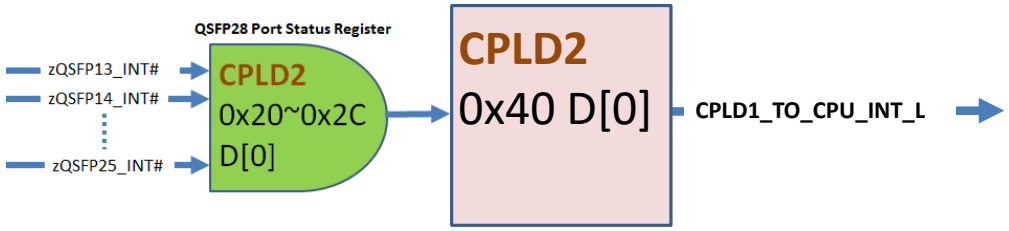
1.9.1 CPLD1 Interrupt

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

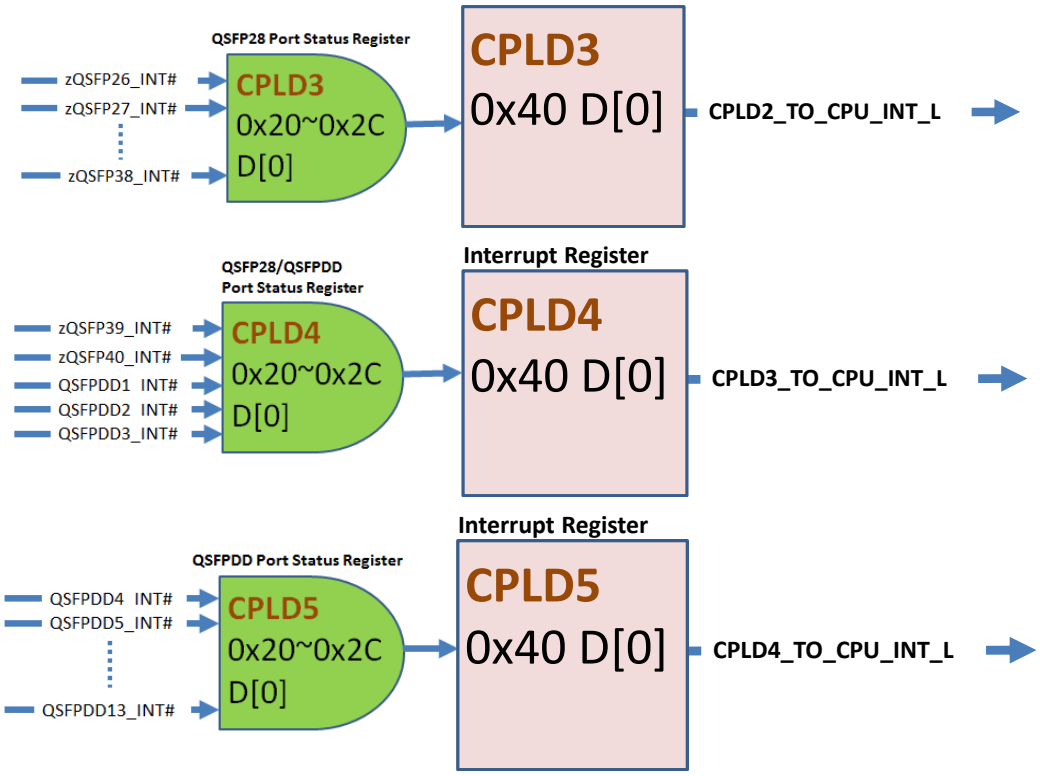




1.9.2 CPLD2/3/4/5 Interrupt



Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved



Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

2 Main System

This section describes in software view to access the system key interfaces in main system.

2.1 Memory and I/O Mapping

Fixed I/O ranges decoded by Broadwell-DE:

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Fixed I/O ranges decoded by Broadwell-DE:

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	6	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	1 6	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	3	SMB unit
TCO	96 bytes above ACPI base	3	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	3	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Memory decode ranges from processor perspective:

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh	LPC or SPI (or PCI)	Always enabled.
FF70 0000h–FF7F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
4 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
1 KB anywhere in 4 GB	USB EHCI Controller #1	Enable using standard PCI mechanism
64 KB anywhere in 4 GB	USB xHCI Controller	Enable using standard PCI mechanism
FED0 X000h–FED0 X3FFh	High Precision Event	BIOS determines “fixed” location which is

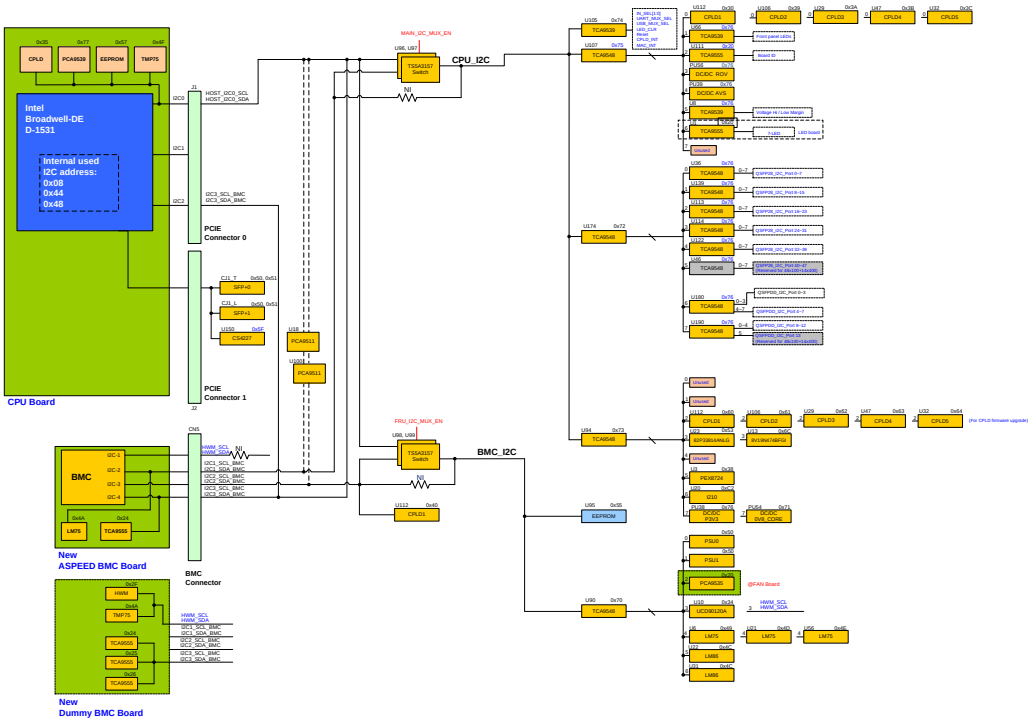
Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit	PCI Bridge	Enable using standard PCI mechanism
Prefetchable Memory	PCI Bridge	Enable using standard PCI mechanism
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic
32 Bytes anywhere in 64-bit	SMBus	Enable using standard PCI mechanism
2 KB anywhere above 64 KB	SATA Host Controller #1	AHCI memory-mapped registers. Enable
Memory Base/Limit	PCI Express* Root Ports 1-	Enable using standard PCI mechanism
Prefetchable Memory	PCI Express Root Ports 1-8	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
16 Bytes anywhere in 64-bit	Intel® MEI #1, #2	Enable using standard PCI mechanism
4 KB anywhere in 4 GB	KT	Enable using standard PCI mechanism
16 KB anywhere in 4 GB	Root Complex Register	Enable using setting bit[0] of the Root

2.1.1 SMbus

There is one SMbus, which is I2C compatible, on S9500-30XS controlled by CPU card. It is configured to operate in standard mode, 100KHz clock frequency. Four I2C buses from BMC are connected to switch board I2C devices with dedicated I2C mux.

I2C block diagram is shown as below:



Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

CPU_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CPU_I2C	I/O EXP	111-0100	0x74	TCA9539	0.7	8V19N474_INT
					0.6	UART_MUX1_SEL
					0.5	UART_MUX2_SEL
					0.4	USB_MUX_SEL
					0.3	HOST_TO_BMC_I2C_GPIO
					0.2	LED_CLR
					0.1	EXP_J2_PCIE_RST_L
					0.0	9539_J2_RST_L
					1.7	I210_RST_L
					1.6	I210_PE_RST_L
					1.5	OP2_INT_L
					1.4	CPLD01_TO_CPU_INT_L
					1.3	CPLD2_TO_CPU_INT_L
					1.2	CPLD3_TO_CPU_INT_L
					1.1	CPLD4_TO_CPU_INT_L
					1.0	J2_INT_L
	I2C MUX	111-0001	0x75	TCA9548	--	CPLDs, System LEDs, Board ID, CPLDs DC/DC ROV, DC/DC AVS, Voltage Margin
	I2C MUX	111-0010	0x72	TCA9548	--	I2C of QSFP28 Port 1~40 I2C of QSFPDD Port 1 ~13
	I2C MUX	111-0011	0x73	TCA9548	--	CPLD upgrade Clock Gens. PCIE switch, PEX8716 Ethernet controller, I210 DC/DC P3V3, DC/DC 0V8_CORE
	Device				**Ch #**	**Function**
	TCA9548 0x75				Ch0	CPLD1~CPLD5 , 0x40, 0x39 ~ 0x3C
					Ch1	TCA9539, 0x76 Ch1.7: Unused Ch1.6: Unused Ch1.5: Unused Ch1.4: Unused Ch1.3: Unused Ch1.2: Unused Ch1.1: PSU0_PWROK

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

I2C Bus	Name	Address		Device	Bit #	Function
						Ch1.0: PSU1_PWROK Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: PSU0_LED_Y Ch0.3: PSU1_LED_Y Ch0.2: FAN_LED_Y Ch0.1: FAN_LED_EN Ch0.0: PSU0_LED_Y
					Ch2	TCA9555, 0x20 Ch1.7: Board_ID_3 Ch1.6: Board_ID_2 Ch1.5: Board_ID_1 Ch1.4: Board_ID_0 Ch1.3: HW_REV_1 Ch1.2: HW_REV_0 Ch1.1: Build_REV_1 Ch1.0: Build_REV_0 Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: Unused Ch0.3: Unused Ch0.2: Unused Ch0.1: Unused Ch0.0: Unused
					Ch3	DC/DC ROV, 0x76
					Ch4	DC/DC AVS, 0x76
					Ch5	TCA9539, 0x76 Voltage High/Low margin test
					Ch6	TCA9548, 0x20 Beacon LED
					Ch7	Unused
	Device				**Ch #**	**Function**
	TCA9548 0x72				Ch0	TCA9548, 0x76 Ch0: QSFP28 Port 0 I2C Ch1: QSFP28 Port 1 I2C Ch2: QSFP28 Port 2 I2C Ch3: QSFP28 Port 3 I2C Ch4: QSFP28 Port 4 I2C Ch5: QSFP28 Port 5 I2C Ch6: QSFP28 Port 6 I2C Ch7: QSFP28 Port 7 I2C

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

I2C Bus	Name	Address		Device	Bit #	Function
					Ch1	TCA9548, 0x76 Ch0: QSFP28 Port 8 I2C Ch1: QSFP28 Port 9 I2C Ch2: QSFP28 Port 10 I2C Ch3: QSFP28 Port 11 I2C Ch4: QSFP28 Port 12 I2C Ch5: QSFP28 Port 13 I2C Ch6: QSFP28 Port 14 I2C Ch7: QSFP28 Port 15 I2C
					Ch2	TCA9548, 0x76 Ch0: QSFP28 Port 16 I2C Ch1: QSFP28 Port 17 I2C Ch2: QSFP28 Port 18 I2C Ch3: QSFP28 Port 19 I2C Ch4: QSFP28 Port 20 I2C Ch5: QSFP28 Port 21 I2C Ch6: QSFP28 Port 22 I2C Ch7: QSFP28 Port 23 I2C
					Ch3	TCA9548, 0x76 Ch0: QSFP28 Port 24 I2C Ch1: QSFP28 Port 25 I2C Ch2: QSFP28 Port 26 I2C Ch3: QSFP28 Port 27 I2C Ch4: QSFP28 Port 28 I2C Ch5: QSFP28 Port 29 I2C Ch6: QSFP28 Port 30 I2C Ch7: QSFP28 Port 31 I2C
					Ch4	TCA9548, 0x76 Ch0: QSFP28 Port 32 I2C Ch1: QSFP28 Port 33 I2C Ch2: QSFP28 Port 34 I2C Ch3: QSFP28 Port 35 I2C Ch4: QSFP28 Port 36 I2C Ch5: QSFP28 Port 37 I2C Ch6: QSFP28 Port 38 I2C Ch7: QSFP28 Port 39 I2C
					Ch5	TCA9548, 0x76 Ch0: Reserved for QSFP28 Port 40 I2C Ch1: Reserved for QSFP28 Port 41 I2C Ch2: Reserved for QSFP28 Port 42 I2C Ch3: Reserved for QSFP28 Port 43 I2C Ch4: Reserved for QSFP28 Port 44 I2C Ch5: Reserved for QSFP28 Port 45 I2C Ch6: Reserved for QSFP28 Port 46 I2C Ch7: Reserved for QSFP28 Port 47 I2C
					Ch6	TCA9548, 0x76 Ch0: QSFPDD Port 0 I2C Ch1: QSFPDD Port 1 I2C Ch2: QSFPDD Port 2 I2C Ch3: QSFPDD Port 3 I2C Ch4: QSFPDD Port 4 I2C

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

I2C Bus	Name	Address		Device	Bit #	Function
						Ch5: QSFPDD Port 5 I2C Ch6: QSFPDD Port 6 I2C Ch7: QSFPDD Port 7 I2C
					Ch7	TCA9548, 0x76 Ch0: QSFPDD Port 8 I2C Ch1: QSFPDD Port 9 I2C Ch2: QSFPDD Port 10 I2C Ch3: QSFPDD Port 11 I2C Ch4: QSFPDD Port 12 I2C Ch5: Reserved for QSFPDD 13 Ch6: Unused Ch7: Unused
	Device				**Ch #**	**Function**
	TCA9548 0x73				Ch0	Unused
					Ch1	Unused
					Ch2	CPLD1~CPLD5, 0x60~0x64 For CPLD firmware upgrade
					Ch3	Clock generators 82P33814ANLG, 0x53 8V19N474BFGI, 0x6C
					Ch4	Unused
					Ch5	PCIE Switch PEX8724, 0x38
					Ch6	Ethernet Controller I210, 0xC2
					Ch7	DC/DC P3V3, 0x76 DC/DC 0V8_CORE, 0x71

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

BMC_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
BMC_I2C	EEPROM	101-0101	0x55	M24128	--	Main Board EEPROM
	CPLD1	000-0100	0x40	CPLD	--	CPLD1
	I2C MUX	111-0000	0x70	TCA9548	--	FRU units, thermal sensors
	Device				**Ch #**	**Function**
	TCA9548 0x74				Ch0	PSU0, 0x50
					Ch1	PSU1, 0x50
					Ch2	PCA9535, 0x20 (at Fan board) Ch1.7: FAN4_DIR Ch1.6: FAN4_ABS Ch1.5: FAN4_LED_Y Ch1.4: FAN4_LED_G Ch1.3: FAN3_DIR Ch1.2: FAN3_ABS Ch1.1: FAN3_LED_Y Ch1.0: FAN3_LED_G Ch0.7: FAN2_DIR Ch0.6: FAN2_ABS Ch0.5: FAN2_LED_Y Ch0.4: FAN2_LED_G Ch0.3: FAN1_ABS Ch0.2: FAN1_ABS Ch0.1: FAN1_LED_Y Ch0.0: FAN1_LED_G
					Ch3	Voltage monitor UCD90120A, 0x34 HWM W83795, 0x2F
					Ch4	Thermal sensor LM75, 0x49 Thermal sensor LM75, 0x4D Thermal sensor LM75, 0x4E
					Ch5	Thermal sensor LM86, 0x4C
					Ch6	Thermal sensor LM86, 0x4C
					Ch7	reserved

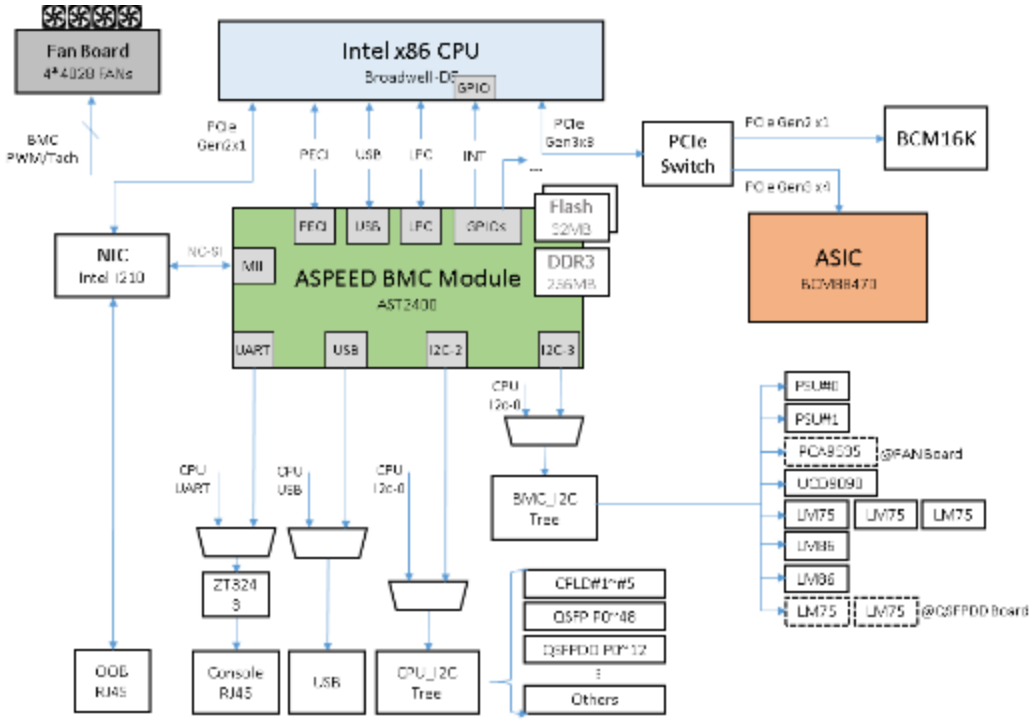
CS4227_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CS4227_I2C	SFP+0	101-0000 101-0001	0x50 0x51	SFP+	--	SFP+ Port 0
	SFP+1	101-0000 101-0001	0x50 0x51	SFP+	--	SFP+ Port 1

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

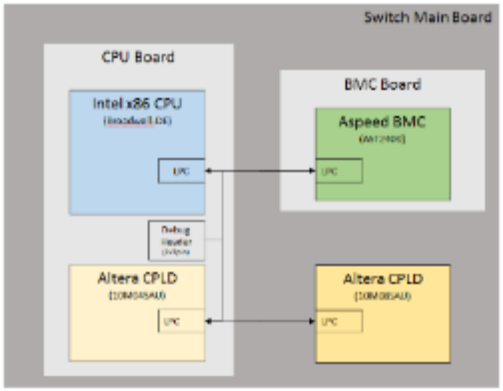
3 BMC sub-system

In S9700-53DX project, base board management controller (BMC) autonomous monitors system's health including temperature, voltage, fan speed, etc. We use the DDR4 SO-DIMM connector as the BMC module connector. The BMC module connector is on the main board PCBA.:



3.1 LPC

Low-Pin-Count interface is an important interface for communication among Broadwell-DE, CPLD on CPU Board and BMC. The OS running in x86 use this interface to communicate with BMC's IPMI message handler. The connection topology is shown as below.



Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

3.2 GPIO

AST2400 Integrates one set of Parallel GPIO Controller with maximum 216 control pins, which are 28 sets, to provide general-purpose input/output functions. All functional parallel GPIOs of S9700-53DX router in different group are listed as below.

Group	Ball Name	Net Name	Direction	Function
GPIOB	GPIOB0	THERMAL_ALERT	input	Interrupt to BMC for thermal event
	GPIOB4	CPU_TH_RST_L	output	Reset of BCM88690
GPIOE	GPIOE2	PSU1_PWRON_L	input	PSU#0 Power On signal
	GPIOE3	BMC_TO_UCD_RST_L	output	Reset from BMC to UCD
GPIOF	GPIOF3	CPU_PRSNT_L	input	CPU card present signal
	GPIOF5	USB_MUX_SEL	output	USB Switch for CPU or BMC
GPIOK	GPIOK0	UART_MUX_SEL	output	Uart switch for CPU or BMC
	GPIOK1	P3V3_FAN_EN	output	Fan enable
	GPIOK2	FAN_STATUS_INT_L	input	Fan status interrupt
	GPIOK3	FP_BTN_UARTSEL_EN_L	output	Front panel uart switch
	GPIOK4	RST_CPU_PWRBTN_N	output	Reset from BMC to CPU
	GPIOK5	ALL_PWR_GOOD	input	All power good on BMC module card
	GPIOK6	PSU0_PRSNT_N	input	PSU#0 present signal
	GPIOK7	PSU0_PWROK	input	PSU#0 Power OK signal
GPIOL	GPIOL2	SYSTEM_LED_RST_L	input	System LED reset control
	GPIOL3	HOST_TO_BMC_I2C_GPIO	input	Reserved GPIO between CPU and BMC
	GPIOL4	MAIN_I2C_MUX_RST_L	input	I2C Switch for CPU or BMC
GPIOM	GPIOM0	HOST_TO_BMC_INT_L	input	Interrupt from CPU to BMC
	GPIOM1	BMC_TO_HOST_NMI	output	Interrupt from BMC to CPU
	GPIOM2	RST_BMC_TO_CPU_N	output	Reset from BMC to CPU
	GPIOM4	P3V3_I2C_EN	output	I2C tree power enable

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

	GPIOM6	UCD9090_INT_L	input	Interrupt from UCD to BMC
	GPIOM7	UCD9090_CNTRL	output	UCD enable signal
GPIOP	GPIOP2	PSU0_PWRON_L	input	PSU#0 power OK signal
	GPIOP3	PSU0_INT_L	input	PSU#0 interrupt
	GPIOP4	PSU1_PWRON_L	input	PSU#1 power On signal
	GPIOP5	PSU1_PWROK	input	PSU#1 power OK signal
	GPIOP6	BMC_INT	output	Interrupt from BMC to CPU
	GPIOP7	PSU1_INT_L	input	PSU#1 interrupt

3.3 Base Board Management

BMC starts to configure, manage and monitor components through I2C, LPC, NC-SI interfaces. The following table lists these components and actions.

Interface	Component	IPMI device name	Configure
[0x74] I2C MUX TCA9548 #0	[0x50] PSU0_MCU	PSU0_FAN	Get speed
		PSU0_Temp	Get temperature/Set threshold value
	[0x50] PSU1_MCU	PSU1_FAN	Get speed
		PSU1_Temp	Get temperature/Set threshold value
	[0x20] PCA9535@FAN Board (FAN direction)	-	Get FAN direction
	[0x34] UCD90120	PERI_P3V3_VIN	Get voltage/Set threshold value
		P5V_SB_VIN	Get voltage/Set threshold value
		P3V8_BMC_VIN	Get voltage/Set threshold value
		P2V5_VIN	Get voltage/Set threshold value
		P3V3_BMC_VIN	Get voltage/Set threshold value
		ROV_CORE_VIN	Get voltage/Set threshold value
		P1V8_VIN	Get voltage/Set threshold value
		P1V2_VIN	Get voltage/Set threshold value
		P0V9_VIN	Get voltage/Set threshold value
		P0V88_VIN	Get voltage/Set threshold value

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

		AVS_CORE_MON	Get voltage/Set threshold value
		0V8_CORE_MON	Get voltage/Set threshold value
	[0x49] LM75@ Main Board	Temp_BOARD1	Get temperature/Set threshold value
	[0x4D] LM75@ Main Board	Temp_BOARD2	Get temperature/Set threshold value
	[0x4E] LM75@ Main Board	Temp_BOARD3	Get temperature/Set threshold value
	[0x4C] LM86@ Main Board	Temp_MAC1	Get temperature/Set threshold value
	[0x4C] LM86@ Main Board	Temp_MAC2	Get temperature/Set threshold value
	[0x4D] LM75@QSFPDD	Temp_QSFP1	Get temperature/Set threshold value
	[0x4E] LM75@QSFPDD	Temp_QSFP2	Get temperature/Set threshold value
TACHO	TACHO#1 @bmc card	Fan0	Get speed
	TACHO#3 @bmc card	Fan1	Get speed
	TACHO#5 @bmc card	Fan2	Get speed
	TACHO#7 @bmc card	Fan3	Get speed
PECI	PECI	TEMP_CPU_PECI	Get temperature/Set threshold value
ADC	BMC integrated ADC #0	P3V15_LICELL	Get voltage/Set threshold value
	BMC integrated ADC #1	ADC_CPU_TEMP_SENSOR	Get temperature/Set threshold value
	BMC integrated ADC #2	HWM_VDD_CORE_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #4	HWM_P1V8_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #5	P3V3_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #6	HWM_P0V8_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #12	BMC_P1V26_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #13	BMC_P1V538_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #14	BMC_P3V3_VSENSE	Get voltage/Set threshold value
	BMC integrated ADC #15	BMC_P5V_VSENSE	Get voltage/Set threshold value

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

4 CPLD

4.1 CPU board CPLD Register Mapping and Description

Offset	Register	Description
0x00	Revision	Revision register
0x01	Status-0	Status register for reading input signals from BMC
0x02	Status-1	Status register for reading information of BIOS flash selection
0x03	Cntrl-0	Control register used to send signals to BMC
0x04	Cntrl-1	Control register used to send signals to BMC
0x05	Mask-0	
0x06	SKU ID	SKU ID register

CPU CPLD resistor description is shown as below:

Revision				
Offset = 0x00				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7:4	RO	Revision	0000	CPLD Revision Number, hardwired
3:0	RO	Revision	1011	CPLD Revision Number, hardwired

Status-0				
Offset = 0x01				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	R/W	BMC_to_HOST_NMI_L	1	Non-maskable Interrupt Request to BMC
6	R/W	BMC_to_HOST_INT_L	1	Interrupt Request to BMC
5:0		Reserved	X	

Status-1				
Offset = 0x02				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	RO	BIOS_MUXSEL	x	Actual value of BIOS_MUXSEL. If the Watchdog logic triggered, it will be different than CTRL-1[7]. Otherwise, it will be same value.
6:0		Reserved	X	

Cntrl-0				
Offset = 0x03				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	R/W	HOST_to_MB_RST_L	1	Reset signal to reset the motherboard from CPU
6	R/W	HOST_to_MB_I2C_RST_L	1	
5	R/W	HOST_to_BMC_RST_L	1	
4	R/W	HOST_to_MM_INT_L	1	
3:0		Reserved	x	

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

Cntrl-1				
Offset = 0x04				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	R/W	BIOS_MUX_SEL	0	This bit is not reset with a hardware reset. It will default to its value when power up, only. This value is used to write to the BIOS MUX selector when watchdog recovery is disabled (WDT_RCVRY_EN=0).
6:1		Reserved	x	
1	R/W	WDT_DOG_EN	1	This bit enables the Watchdog timer during boot process. The CPU must disable this bit right after it boots. It is enabled upon power up or sys_reset.
0	R/W	WDT_RCVRY_EN	1	This bit enables the watchdog recovery logic. It controls bios_mux_sel

Mask-0				
Offset = 0x05				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	R/W	Reserved	X	
6	R/W	BMC_to_HOST_INT_Mask	1	Mask to disable BMC-to-Host Interrupt.
5:1		Reserved	X	
0	R/W	TH_RESET_MASK	1	Mask to disable cpld_pcie_reset_n going to motherboard.

SKU ID				
Offset = 0x06				
Bit	**R/W**	**Name**	**Reset Value**	**Description**
7	RO	SKU_ID3	0	SKU ID[3:0] = 0000 0000 : Apache BW-DE CPU board 0001 : Reserved 0010 : Reserved : 1111 : Reserved
6	RO	SKU_ID2	0	
5	RO	SKU_ID1	0	
4	RO	SKU_ID0	0	
3	RO	HW_REV_ID1	1	Hardware Revision [1:0]= 10 00: Proto 01: Alpha 10: Beta 11: PVT
2	RO	HW_REV_ID0	1	
1	RO	BUILD_ID1	0	Build ID [1:0] = 00 00 : 1 01 : 2 10 : 3 11 : 4
0	RO	BUILD_ID0	0	

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Ufi Space Co., Ltd.
3F.,No.109, Jhongcheng Rd.,Tucheng Dist.,
New Taipei City 23674, Taiwan
Tel : +886-2-5572-4260
Fax : +886-2-5572-4261

4.2 Main board CPLD Register Mapping and Description

CPLD1

Group	Offset	Register Name
Board information	0x00	Board Type and Revision
	0x01	Extend Board Type
	0x02	CPLD Revision Register
	0X03	CPLD ID Register
Port status	x-> QSFP28 Port z 0x30-> QSFP28 P1 …… …… …… 0x3B-> QSFP28 P12	QSFP28 Port Status Register (Address 0x20~2B) (x / z)： (0x30 / 1)、(0x31 / 2) 、(0x32 / 3) (0x33 / 1)、(0x34 / 2) 、(0x35 / 3) (0x36 / 1)、(0x37 / 2) 、(0x38 / 3) (0x39 / 1)、(0x3A / 2) 、(0x3B / 3)
	0x2F	SFP+ Port0/1 Status Register
Port config	x-> QSFP28 Port z 0x30-> QSFP28 P1 …… …… …… 0x3B-> QSFP28 P12	QSFP28 Port Model Select Register (Address 0x30~3B) (x / z)： (0x30 / 1)、(0x31 / 2) 、(0x32 / 3) (0x33 / 1)、(0x34 / 2) 、(0x35 / 3) (0x36 / 1)、(0x37 / 2) 、(0x38 / 3) (0x39 / 1)、(0x3A / 2) 、(0x3B / 3)
	0x3F	SFP+ Port0/1 Configuration Register
	0x40 / 0x41	Interrupt
	0x42	BMC Status
	0x44	Power Status
	0x45	MUX control
	0x49	CPU/BMC Mux circuit setting
	0x4A	Reset Control
	0x4D / 0x4E	Reset Control with pulse output

Board Type and Revision				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x00	D[1:0]	00	RO	Build REV [1:0] 00: P1, A1, B1, etc. 01: P2, A2, B2, etc. 10: P3, A3, B3, etc. 11: P4, A4, B4, etc.

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Board Type and Revision				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3:2]	00	RO	HW REV[1:0]Hardware Revision, defined by external resistors 00: Proto 01: Alpha 10: Beta 11: PVT
	D[7:4]	0000	RO	Model ID [3:0] 0010: S9700-53DX others: Reserved

Extended Board Type				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x01	D[3:0]	0011	RO	Board ID [3:0] 0000~1111: Reserved for extended Board ID
	D[7:4]	0000	RO	Reserved

CPLD Revision Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[5:0]	000000	RO	CPLD code Revision Bit[5:0]: 000000: CPLD Code Revision is X.00 000001: CPLD Code Revision is X.01 000010: CPLD Code Revision is X.02 000011: CPLD Code Revision is X.03 … 111111: CPLD Code Revision is X.63
	D[6]	0	RO	Release Bit: 0: CPLD Code is RD Revision 1: CPLD Code is Release Revision
	D[7]	0	RO	Reserved

CPLD ID Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[2:0]	000	RO	CPLD ID 000: CPLD 1 001: CPLD 2 010: CPLD 3 011: CPLD 4 100: CPLD 5
	D[7:3]	00000	RO	Reserved

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

QSFP28 Port Status Register (Address 0x20~2B)				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
Address mapping : 0x20-> QSFP28 P1 0x21-> QSFP28 P2 0x22-> QSFP28 P3 0x23-> QSFP28 P4 0x24-> QSFP28 P5 0x25-> QSFP28 P6 0x26-> QSFP28 P7 0x27-> QSFP28 P8 0x28-> QSFP28 P9 0x29-> QSFP28 P10 0x2A-> QSFP28 P11 0x2B-> QSFP28 P12	D[0]	1	RO	port A QSFP+/QSFP28 status 1= Port interrupt exist 0= Port interrupt not exist
	D[1]	1	RO	Port A QSFP+/QSFP28Present status 1=Absent 0=Present
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

SFP+ Port0/1 Status Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x2f	D[0]	1	RO	SFP+0 Present status 1=Absent 0=Present
	D[1]	1	RO	SFP+0 TX_Fault status 0=Normal 1=Tx fault
	D[2]	1	RO	SFP+ 0 RX_LOS status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[3]	1	RO	Reserved
	D[4]	1	RO	SFP+0 Present status 1=Absent 0=Present
	D[5]	1	RO	SFP+0 TX_Fault status 0=Normal 1=Tx fault
	D[6]	1	RO	SFP+ 0 RX_LOS status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[7]	1	RO	Reserved

QSFP28 Port Model Select Register (Address 0x30~3B)				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
Address mapping : 0x30-> QSFP28 P0	D[0]	1	RW	Port A QSFP+/QSFP28 RST# status 0:reset QSFP+ module

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

QSFP28 Port Model Select Register (Address 0x30~3B)				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x31-> QSFP28 P1 0x32-> QSFP28 P2 0x33-> QSFP28 P3 0x34-> QSFP28 P4 0x35-> QSFP28 P5 0x36-> QSFP28 P6 0x37-> QSFP28 P7 0x38-> QSFP28 P8 0x39-> QSFP28 P9 0x3A-> QSFP28 P10 0x3B-> QSFP28 P11				1: reset negated
	D[1]	1	RW	Reserved
	D[2]	0	RW	Port A QSFP+/QSFP28 LPMODE status 1= Low Power mode 0= High Power mode
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

SFP+ Port0 Configuration Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x3f	D[0]	0	RW	SFP+0 TXDIS status 0=Operating normally 1=Turned off
	D[1]	1	RW	controls the receive path signal rate capability 0: RX signal rate less than or equal to 4.25 GBd 1: RX signal rate greater than 4.25 GBd
	D[2]	1	RW	controls the transmit path signal rate capability 0: TX signal rate less than or equal to 4.25 GBd 1: TX signal rate greater than 4.25 GBd
	D[3]	1	RW	Reserve
	D[4]	0	RW	SFP+0 TXDIS status 0=Operating normally 1=Turned off
	D[5]	1	RW	controls the receive path signal rate capability 0: RX signal rate less than or equal to 4.25 GBd 1: RX signal rate greater than 4.25 GBd
	D[6]	1	RW	controls the transmit path signal rate capability 0: TX signal rate less than or equal to 4.25 GBd 1: TX signal rate greater than 4.25 GBd
	D[7]	1	RW	Reserved

Interrupt Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[0]	1	RO	Port Interrupt

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Interrupt Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x40				0= Port interrupt exist 1= Port interrupt not exist
	D[1]	1	RO	Gearbox Interrupt 0 : Interrupt Present 1 : Interrupt Absent
	D[2]	0	RO	USB Over Current Protect 0 : USB is no Over current 1 : USB is over current
	D[3]	1	RO	Reserved
	D[4]	1	RO	PSU0 Interrupt 0= Interrupt exist 1= Interrupt not exist
	D[5]	1	RO	PSU Interrupt 0= Interrupt exist 1= Interrupt not exist
	D[6]	1	RO	PEX8724 Interrupt 0= Interrupt exist 1= Interrupt not exist
	D[7]	1	RO	CS4227 Interrupt 0= Interrupt exist 1= Interrupt not exist

Interrupt Register 2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x41	D[0]	1	RO	Retimer Interrupt 0= Interrupt exist 1= Interrupt not exist
	D[1]	1	RO	QSFP28 Fuse Interrupt 0= Interrupt exist 1= Interrupt not exist
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

BMC Status Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[0]	0	RO	BMC present

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

BMC Status Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x42				0= BMC present 1= BMC absent
	D[6:1]	000000	RO	Reserved
	D[7]	1	RO	Thermal Status 0= Status output/Interrupt happen 1= Normal PS: depend on Thermal IC(U22/U31) setting..

Power Status Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x44	D[0]	0	RO	USB present 0= USB present 1= USB absent
	D[3:1]	000	RO	J2 ROV status
	D[4]	0	RO	PSU0 POWER OK 0= PSU0 power fail 1= PSU0 power ok
	D[5]	0	RO	PSU1 POWER OK 0= PSU1 power fail 1= PSU1 power ok
	D[6]	1	RO	PSU0 present 0= PSU0 present 1= PSU0 absent
	D[7]	1	RO	PSU1 present 0= PSU0 present 1= PSU0 absent

Mux Control Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x45	D[0]	0	RW	SFP0 I2C Mux 0= Disable 1= Enable
	D[1]	0	RW	SFP1 I2C Mux 0= Disable 1= Enable
	D[2]	0	RW	CPU read BMC id path 1 0= Disable 1= Enable

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Mux Control Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	0	RW	CPU read BMC id path 2 0= Disable 1= Enable
	D[5:4]	00	RW	Reserved
	D[6]	0	RW	BMC_MUX_SEL 0: I2C_BMC bus from I2C2_BMC 1: I2C_BMC bus from HOST_I2C0
	D[7]	1	RW	CPU_MUX_SEL 0: I2C_CPU bus from I2C1_BMC 1: I2C_CPU bus from HOST_I2C0

Reset Control Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x4A	D[0]	1	RW	Software Reset 0= Reset system 1= Normal
	D[1]	0	RW	CP2104 Reset 0= Normal 1= Reset CP2104
	D[2]	1	RW	Reserved
	D[3]	1	RW	BMC Reset 0= Reset BMC 1= Normal
	D[4]	1	RW	BMC LPC Reset 0= Reset LPC of BMC 1= Normal
	D[5]	1	RW	I210 Reset 0= Reset I210 1= Normal
	D[7:6]	11	RW	Reserved

Reset Control Register 2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x4D	D[0]	1	RW	OP2 CRST_L Reset 0= Reset OP2 CRST_L 10mS 1= Normal
	D[1]	1	RW	OP2 PERST Reset 0= Reset OP2 PERST_L 110mS 1= Normal
	D[2]	1	RW	OP2 SRST_L Reset

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Reset Control Register 2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
				0= Reset OP2 SRST_L 10mS 1= Normal
	D[3]	0	RW	82P33814 Reset 0= Reset 82P33814 80mS 1= Normal Reference: CPLD_RESET_N
	D[4]	0	RW	CS4227 Reset 0= Reset CS4227 2mS 1= Normal
	D[5]	1	RW	Gearbox Reset 0= Reset Gearbox 10mS 1= Normal
	D[6]	1	RW	Reserved
	D[7]	0	RW	PEX8724 Reset 0= Reset PEX8724 10mS 1= Normal Reference: RST_PCIE_CPU_TO_MB_N

Reset Control Register 3				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x4E	D[0]	1	RW	Retimer Reset 0= Reset RST_RETIMER_L 35mS 1= Normal
	D[1]	1	RW	Reserved
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

CPLD2/3/4/5

Group	Offset	Register Name
Board information	0x02	CPLD Revision Register
	0X03	CPLD ID Register

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Group	Offset	Register Name
Port status	0x20-> QSFP28 P13/26/39 (2/3/4) 0x20-> QSFPDD P4 (5) 0x21-> QSFP28 P14/27/40 (2/3/4) 0x21-> QSFPDD P5 (5) 0x22-> QSFP28 P15/28/41 (2/3/4) 0x22-> QSFPDD P6 (5) 0x23-> QSFP28 P16/29/42 (2/3/4) 0x23-> QSFPDD P7 (5) 0x24-> QSFP28 P17/30/43 (2/3/4) 0x24-> QSFPDD P8 (5) 0x25-> QSFP28 P18/31/44 (2/3/4) 0x25-> QSFPDD P9 (5) 0x26-> QSFP28 P19/32/45 (2/3/4) 0x26-> QSFPDD P10 (5) 0x27-> QSFP28 P20/33/46 (2/3/4) 0x27-> QSFPDD P11 (5) 0x28-> QSFP28 P21/34/47 (2/3/4) 0x28-> QSFPDD P12 (5) 0x29-> QSFP28 P22/35/48 (2/3/4) 0x29-> QSFPDD P13 (5) 0x2A-> QSFP28 P23/36 (2/3) 0x2A-> QSFPDD P1 (4) 0x2A-> QSFPDD P14 (5) 0x2B-> QSFP28 P24/37 (2/3) 0x2B-> QSFPDD P2 (4) 0x2C-> QSFP28 P25/38 (2/3) 0x2C-> QSFPDD P3 (4)	QSFP28/QSFPDD Port Status Register (Address 0x20~2C) (2/3/4): CPLD2/3/4 (2/3): CPLD2/3 (4): CPLD4 (5): CPLD5

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Group	Offset	Register Name
Port configuration	0x30-> QSFP28 P13/26/39 (2/3/4) 0x30-> QSFPDD P4 (5) 0x31-> QSFP28 P14/27/40 (2/3/4) 0x31-> QSFPDD P5 (5) 0x32-> QSFP28 P15/28/41 (2/3/4) 0x32-> QSFPDD P6 (5) 0x33-> QSFP28 P16/29/42 (2/3/4) 0x33-> QSFPDD P7 (5) 0x34-> QSFP28 P17/30/43 (2/3/4) 0x34-> QSFPDD P8 (5) 0x35-> QSFP28 P18/31/44 (2/3/4) 0x35-> QSFPDD P9 (5) 0x36-> QSFP28 P19/32/45 (2/3/4) 0x36-> QSFPDD P10 (5) 0x37-> QSFP28 P20/33/46 (2/3/4) 0x37-> QSFPDD P11 (5) 0x38-> QSFP28 P21/34/47 (2/3/4) 0x38-> QSFPDD P12 (5) 0x39-> QSFP28 P22/35/48 (2/3/4) 0x39-> QSFPDD P13 (5) 0x3A-> QSFP28 P23/36 (2/3) 0x3A-> QSFPDD P1 (4) 0x3A-> QSFPDD P14 (5) 0x3B-> QSFP28 P24/37 (2/3) 0x3B-> QSFPDD P2 (4) 0x3C-> QSFP28 P25/38 (2/3) 0x3C-> QSFPDD P3 (4)	QSFP28/QSFPDD Port Model Select Register (Address 0x30~3C)
	0x40	Port Interrupt
400G LED Control	0x80-> QSFPDD LED 1、2 0x81-> QSFPDD LED 3、4 0x82-> QSFPDD LED 5、6 0x83-> QSFPDD LED 7、8 0x84-> QSFPDD LED 9、10	QSFPDD LED control Register (Address 0x80~86) Only for CPLD5

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Group	Offset	Register Name
	0x85-> QSFPDD LED 11、12 0x86-> QSFPDD LED 13、14	

CPLD Revision Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[5:0]	000000	RO	CPLD code Revision Bit[5:0]: 000000: CPLD Code Revision is X.00 000001: CPLD Code Revision is X.01 000010: CPLD Code Revision is X.02 000011: CPLD Code Revision is X.03 … 111111: CPLD Code Revision is X.63
	D[6]	0	RO	Release Bit: 0: CPLD Code is RD Revision 1: CPLD Code is Release Revision
	D[7]	0	RO	Reserved

CPLD ID Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x03	D[2:0]	001	RO	CPLD ID 000: CPLD 1 001: CPLD 2 010: CPLD 3 011: CPLD 4 100: CPLD 5
	D[7:3]	00000	RO	Reserved

QSFP28/QSFPDD Port Status Register (Address 0x20~2C) for CPLD2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x20-> QSFP28 P12 0x21-> QSFP28 P13 0x22-> QSFP28 P14 0x23-> QSFP28 P15 0x24-> QSFP28 P16 0x25-> QSFP28 P17 0x26-> QSFP28 P18 0x27-> QSFP28 P29 0x28-> QSFP28 P20 0x29-> QSFP28 P21 0x2A-> QSFP28 P22 0x2B-> QSFP28 P23	D[0]	1	RO	Port x QSFP28/QSFPDD status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x QSFP28/QSFPDD Present status 1=Absent 0=Present
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

QSFP28/QSFPDD Port Status Register (Address 0x20~2C) for CPLD2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x2C-> QSFP28 P24	D[7]	1	RO	Reserved

QSFP28/QSFPDD Port Status Register (Address 0x20~2C) for CPLD3				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x20-> QSFP28 P25 0x21-> QSFP28 P26 0x22-> QSFP28 P27 0x23-> QSFP28 P28 0x24-> QSFP28 P39 0x25-> QSFP28 P30 0x26-> QSFP28 P31	D[0]	1	RO	Port x QSFP28/QSFPDD status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x QSFP28/QSFPDD Present status 1=Absent 0=Present
0x27-> QSFP28 P32	D[2]	1	RO	Reserved
0x28-> QSFP28 P33	D[3]	1	RO	Reserved
0x29-> QSFP28 P34	D[4]	1	RO	Reserved
0x2A-> QSFP28 P35	D[5]	1	RO	Reserved
0x2B-> QSFP28 P36	D[6]	1	RO	Reserved
0x2C-> QSFP28 P37	D[7]	1	RO	Reserved

QSFP28/QSFPDD Port Status Register (Address 0x20~2C) for CPLD4				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x20-> QSFP28 P38 0x21-> QSFP28 P39 0x22-> QSFP28 P40 0x23-> QSFP28 P41 0x24-> QSFP28 P42 0x25-> QSFP28 P43 0x26-> QSFP28 P44	D[0]	1	RO	Port x QSFP28/QSFPDD status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x QSFP28/QSFPDD Present status 1=Absent 0=Present
0x27-> QSFP28 P45	D[2]	1	RO	Reserved
0x28-> QSFP28 P46	D[3]	1	RO	Reserved
0x29-> QSFP28 P47	D[4]	1	RO	Reserved
0x2A-> QSFPDD P0	D[5]	1	RO	Reserved
0x2B-> QSFPDD P1	D[6]	1	RO	Reserved
0x2C-> QSFPDD P2	D[7]	1	RO	Reserved
QSFP28/QSFPDD Port Status Register (Address 0x20~2A) for CPLD5				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x20-> QSFPDD P4 0x21-> QSFPDD P5 0x22-> QSFPDD P6 0x23-> QSFPDD P7 0x24-> QSFPDD P8 0x25-> QSFPDD P9 0x26-> QSFPDD P10 0x27-> QSFPDD P11 0x28-> QSFPDD P12	D[0]	1	RO	Port x QSFP28/QSFPDD status 1= Transceiver's optical side link down 0= Transceiver's optical side link up
	D[1]	1	RO	Port x QSFP28/QSFPDD Present status 1=Absent 0=Present
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	Reserved

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

QSFP28/QSFPDD Port Status Register (Address 0x20~2C) for CPLD4				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x29-> QSFPDD P13 0x2A-> QSFPDD P14	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

QSFP28 Port Model Select Register (Address 0x30~3C) for CPLD2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x30-> QSFP28 P12 0x31-> QSFP28 P13 0x32-> QSFP28 P14	D[0]	1	RW	Port x QSFP28/QSFPDD RST# status 0: reset QSFP+ module 1: reset negated
0x33-> QSFP28 P15	D[1]	1	RW	Reserved
0x34-> QSFP28 P16 0x35-> QSFP28 P17 0x36-> QSFP28 P18 0x37-> QSFP28 P19	D[2]	0	RW	Port x QSFP28/QSFPDD LPMODE status 1= Low Power mode 0= High Power mode
0x38-> QSFP28 P20	D[3]	1	RW	Reserved
0x39-> QSFP28 P21	D[4]	1	RW	Reserved
0x3A-> QSFP28 P22	D[5]	1	RW	Reserved
0x3B-> QSFP28 P23	D[6]	1	RW	Reserved
0x3C-> QSFP28 P24	D[7]	1	RW	Reserved

QSFP28 Port Model Select Register (Address 0x30~3C) for CPLD3				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x30-> QSFP28 P25 0x31-> QSFP28 P26 0x32-> QSFP28 P27	D[0]	1	RW	Port x QSFP28/QSFPDD RST# status 0: reset QSFP+ module 1: reset negated
0x33-> QSFP28 P28	D[1]	1	RW	Reserved
0x34-> QSFP28 P29 0x35-> QSFP28 P30 0x36-> QSFP28 P31 0x37-> QSFP28 P32	D[2]	0	RW	Port x QSFP28/QSFPDD LPMODE status 1= Low Power mode 0= High Power mode
0x38-> QSFP28 P33	D[3]	1	RW	Reserved
0x39-> QSFP28 P34	D[4]	1	RW	Reserved
0x3A-> QSFP28 P35	D[5]	1	RW	Reserved
0x3B-> QSFP28 P36	D[6]	1	RW	Reserved
0x3C-> QSFP28 P37	D[7]	1	RW	Reserved
QSFP28 Port Model Select Register (Address 0x30~3C) for CPLD4				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x30-> QSFP28 P38 0x31-> QSFP28 P39 0x32-> QSFP28 P40	D[0]	1	RW	Port x QSFP28/QSFPDD RST# status 0: reset QSFP+ module 1: reset negated
0x33-> QSFP28 P41	D[1]	1	RW	Reserved

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

QSFP28 Port Model Select Register (Address 0x30~3C) for CPLD3				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x34-> QSFP28 P42 0x35-> QSFP28 P43 0x36-> QSFP28 P44 0x37-> QSFP28 P45	D[2]	0	RW	Port x QSFP28/QSFPDD LPMODE status 1= Low Power mode 0= High Power mode
0x38-> QSFP28 P46	D[3]	1	RW	Reserved
0x39-> QSFP28 P47	D[4]	1	RW	Reserved
0x3A-> QSFPDD P0	D[5]	1	RW	Reserved
0x3B-> QSFPDD P1	D[6]	1	RW	Reserved
0x3C-> QSFPDD P2	D[7]	1	RW	Reserved

QSFP28 Port Model Select Register (Address 0x30~3A) for CPLD5				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x30-> QSFPDD P3 0x31-> QSFPDD P4	D[0]	1	RW	Port x QSFP28/QSFPDD RST# status 0: reset QSFP+ module 1: reset negated
0x32-> QSFPDD P5	D[1]	1	RW	Reserved
0x33-> QSFPDD P6 0x34-> QSFPDD P7 0x35-> QSFPDD P8 0x36-> QSFPDD P9	D[2]	0	RW	Port x QSFP28/QSFPDD LPMODE status 1= Low Power mode 0= High Power mode
0x37-> QSFPDD P10	D[3]	1	RW	Reserved
0x38-> QSFPDD P11	D[4]	1	RW	Reserved
0x39-> QSFPDD P12	D[5]	1	RW	Reserved
0x3A-> QSFPDD P13	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Port Interrupt Register				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x40	D[0]	1	RW	Port Interrupt 0=Port interrupt exist 1= Port interrupt not exist
	D[1]	1	RW	Reserved
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved

Port QSFPDD LED0~LED13 Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x80: Port 0~1 0x81: port 2~3 0x82: Port 4~5 0x83: port 6~7 0x84: Port 8~9 0x85: port 10~11 0x86: Port 12~13	D[0]	0	RW	Port x LED Status 1: Yellow On 0: Yellow Off
	D[1]	0	RW	Port x LED Status 1: Green On 0: Green Off
	D[2]	0	RW	Port x LED Status 1: Blue On 0: Blue Off
	D[3]	0	RW	Port x LED Blinking 1: Blinking 0: keep the Status
	D[4]	0	RW	Port (x+1) LED Status 1: Yellow On 0: Yellow Off
	D[5]	0	RW	Port (x+1) LED Status 1: Green On 0: Green Off
	D[6]	0	RW	Port (x+1) LED Status 1: Blue On 0: Blue Off
	D[7]	0	RW	Port (x+1) LED Blinking 1: Blinking 0: keep the Status

Copyright © 2020 by Ufi Space Co., Ltd. All rights reserved